REMARKS

In the above referenced office action, Claims 1-21 are pending in the application. Claims 1-4, 11-14 and 21 stand rejected. Claims 5-10 and 15-20 are being objected to but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No new matter is being added.

Rejections Under 35 USC § 103(a)

Claims 1-4, 11-14 and 21 have been rejected under 35 USC § 103(a) as being unpatentable over Zheng (U.S. Patent 6,195,303) (hereinafter "Zheng") in view of Tabo (U.S. Patent 6,273,895) (hereinafter "Tabo"). These rejections have been traversed and reconsideration is hereby respectfully requested.

In regards to Claim 1, Claim 1 recites "generating an *address* for a first one of the N memory blocks as a current first possible refresh block and *address for a current second one of the N memory blocks* as a current *second* possible refresh block, for refreshing at least a portion of *one* of the possible refresh blocks" (emphasis added).

The Office Action acknowledges on page 3 that "Zheng does not clearly disclose the step of generating address for a current second one of the N memory blocks as a current second possible refresh block". The Office Action, however, asserts that Tabo teaches "a memory refreshing system having a first memory refresh controller supplying a first refresh request to a memory system to form a first possible refresh block and a

second memory refresh controller supplying a second refresh request to the memory system to form a second possible refresh block".

Zheng teaches various mechanisms for refreshing a DRAM, all of which are based on generating a single address used for refreshing a corresponding portion of the DRAM. Specifically, description for the Ref_Addr Generator (630 in FIG. 6 and 730 in FIG. 7) discloses the generation of the single address as an output. Thus, Zheng does not teach or suggest the generation of two possible selectable addresses for refreshing a portion of one of the possible refresh blocks.

Referring to column 3, lines 1-8 and FIG. 1, Tabo discloses "The *normal refresh circuit (i.e., 200-A) need only transmit a control signal to a memory bank* using the CAS-before-RAS method to provide a refresh cycle for the memory bank. *Inside the memory bank*, an incorporated *refresh address counter* automatically increments an address upon each refresh cycle" (emphasis added). That is, Tabo teaches use of a single control signal for refreshing a corresponding memory bank. Therefore, Tabo does not teach or suggest generating an address for a first one of the N memory blocks and generating an address for a second one of the N memory blocks for checking contention with an externally generated access to one of the N memory blocks.

In addition, Claim 1 also recites "permitting the externally generated access to the one of the N memory blocks *during a certain interval* and refreshing the at least portion of

the current first possible refresh block *during the certain interval* responsive to the memory block of the externally generated access not contending with the current first possible refresh block" (emphasis added).

Referring to column 1, lines 65-67, column 2, lines 42-44, and column 2 lines 49-51, Zheng teaches "The refresh control circuit *initiates refresh of selected memory cells* within the DRAM *in time periods between memory accesses* of the DRAM" (emphasis added). Zheng does not teach or suggest refreshing memory in the same time interval as permitting an external access. With reference to the abstract, Tabo teaches "a first memory refresh controller for supplying a refresh request to the memory system *every first time period*; a second memory refresh controller, provided for each of the memory banks, for supplying a refresh request to the corresponding memory bank *every second time period* that is longer than *the first time period*" (emphasis added). Therefore, Tabo teaches that normal refresh cycles occur only during a first time period and self-refresh cycles occur only during a second time period that is longer than the first time period. In contrast, Claim 1 includes limitations that permit external access and memory refresh to occur within the same time interval.

Therefore, the Office Action fails to establish a *prima facie* case of obviousness, since the Office Action does not point out where each and every element of the claimed invention, arranged as required by Claim 1, is found in one or more prior art references or a combination thereof, either expressly or

under the principles of inherency. Hence, Claim 1 is allowable for at least this reason.

In regards to Claim 2, Claim 2 recites "permitting the externally generated access to the one of the N memory blocks *during a certain interval*, and refreshing the at least portion of the current second possible refresh block *during the certain interval*." (emphasis added). Referring to Column 7, line 17 through Column 8, line 14, and Column 8, lines 29-39, the Office Action states that Zheng teaches or suggests, either expressly or under the principles of inherency, all of the limitations of Claim 2.

Applicants have reviewed above cited reference and are unable to find refreshing of a memory block to occur within the same time interval as permitting the externally generated access to one of the memory blocks. On the contrary, in column 8, lines 29-31, Zheng teaches "The specific embodiment shown in FIG. 6 allows for *either* a memory access *or* a refresh of a set of rows of memory, when enabled, at any particular clock cycle" (emphasis added). In addition, Zheng and Tabo considered individually or in combination, do not teach or suggest comparison of the first and second addresses for checking whether the first and second possible refresh blocks are the same. Hence, Claim 2 is allowable for at least this reason.

In regards to Claims 3 and 4, they directly or indirectly depend from Claim 1. For reasons similar to those stated above in regards to Claim 1, Claims 3 and 4 are allowable for at least this reason.

In regards to Claim 11, Claim 11 recites "a multiplexer for receiving the current first possible refresh block and the current second possible refresh block from the respective address generators". The Office Action states "the limitation of the Claim (11) are rejected as the same reasons set forth in Claim 1."

Zheng does not teach or suggest a multiplexer for receiving inputs from the respective address generators. On the contrary, Zheng discloses a Mux (632 in FIG. 6 and 732 in FIG. 7) to receive only one input from the Ref_Addr Generator (630 in FIG. 6 and 730 in FIG. 7). Similarly, Tabo does not teach or suggest a multiplexer for receiving inputs from the respective address generators. In addition, for reasons similar to those stated in Claim 1, Zheng and Tabo considered individually or in combination do not teach refreshing of a memory block to occur within the same time interval as permitting the externally generated access to one of the memory blocks.

Therefore, the Office Action fails to establish a *prima facie* case of obviousness, since the Office Action does not point out where each and every element of the claimed invention, arranged as required by the Claim 11, is found in one or more prior art references or a combination thereof, either expressly

or under the principles of inherency. Hence, Claim 11 is allowable for at least this reason.

Independent Claim 21 includes limitations similar to those of Claims 1 and 11. Hence, Claim 21 is allowable for reasons similar to those stated above in regards to Claims 1 and 11. Dependent Claims 12, 13 and 14, directly or indirectly depend from Claim 11. Claims 12, 13, and 14 also include additional features not found in the cited reference. For reasons similar to those stated above in regards to Claim 11, Claims 12, 13 and 14 are allowable for at least this reason.

Allowable Subject Matter

Claims 5-10 and 15-20 are being objected to but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Examiner's conditional allowance of Claims 5-10 and 15-20 is appreciated.

Claims 5-10 indirectly or directly depend from Claim 1. Similarly, Claims 15-20 indirectly or directly depend from Claim 11. For reasons similar to those stated above in regards to Claims 1 and 11, Claims 5-10 and 15-20 are allowable in their present form for at least this reason.

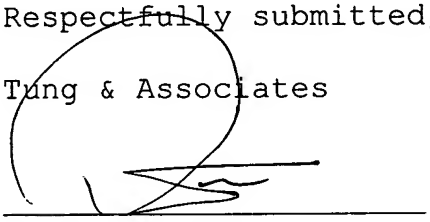
CONCLUSIONS

For the foregoing reasons, the Applicants respectfully submit that the present application is now in condition for allowance. Accordingly, the Examiner is requested to issue a Notice of Allowance for all pending claims.

Should the Examiner deem that any further action by the Applicants would be necessary for placing this application in condition for allowance, the Examiner is invited to contact the undersigned agent at the telephone number listed below.

Respectfully submitted,

Tung & Associates



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